ABSTRACT OF THE DISCLOSURE

A central processing apparatus assigns instructions of a program to a plurality of buffers respectively connected to one of a plurality of execution units. The program consists of a plurality of instruction sequences each including a data dependency. A control dependency between the instruction sequences is represented by a commit instruction. An instruction of data production or data consumption includes a flag representing possession of a register number in a global register accessed by the instruction. A task window number generator assigns a task window number to the instruction sequences in a task window having the commit instruction at the end. Each instruction sequence corresponds to one buffer to assign each instruction of the instruction sequence. A register update unit updates data in the register number accessed by a particular instruction sequence if the particular instruction sequence is accepted by the commit instruction in the task window. A memory update unit updates data in an address of the memory accessed by a particular instruction sequence if the particular instruction sequence is accepted by the commit instruction in the task window.